REMARKS

The Final Office Action dated June 22, 2005, has been received and reviewed.

Claims 1-5, 11-17, 25-28, and 33-38 are currently pending and under consideration in the above-referenced application, each standing rejected.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 103(a)

Claims 1-5, 11-17, 25-28, and 33-38 have been rejected under 35 U.S.C. § 103(a).

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Tsai in View of Lancaster

Claims 1-4, 11-14, 16, 25-27, 33-35, and 37 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over the subject matter taught in U.S. Patent 5,712,185 to Tsai et al. (hereinafter "Tsai"), in view of teachings from U.S. Patent 4,835,584 to Lancaster (hereinafter "Lancaster").

Tsai teaches a process for fabrication isolation structures. The process of Tsai includes forming a trench 38 through a photomask 37, a sacrificial silicon oxide layer 36, a silicon nitride layer 34, and a pad oxide layer 32, and into a silicon substrate 30, as shown in FIGs. 3C and 3D. *See also* col. 2, line 53, to col. 3, line 18. Once the trench 38 is formed, the photomask 37 is removed and the edges of the remainder of the silicon nitride layer 34A are etched back, as depicted by FIG. 3E. *See also* col. 3, lines 9 and 19-33. Thereafter, exposed silicon at the

surfaces of the trench 38A is oxidized to form side wall oxidation 39. FIG. 3F; col. 3, lines 34-38. The side wall oxidation 39 relieves defects that are formed in the silicon substrate 30 as the edges of the silicon nitride layer 34A are etched back. Col. 3, lines 34-37.

The teachings of Lancaster are directed to a process for forming a transistor within a trench. That process includes forming an oxide lining 52a within trenches 56 that extend into a silicon substrate 50. FIG. 5D; col. 3, lines 43-45. The oxide lining 52a is purportedly formed to protect the silicon substrate 50 as a silicon nitride mask layer 53 is subsequently removed. Col. 3, lines 39-49; FIG. 5E. Notably, the *entire* silicon nitride mask layer 53 is removed. *Id.* The oxide lining 52a, which is included merely for the sake of providing etch selectivity to prevent enlargement of the trenches 56 during removal of the silicon nitride mask layer 53 (col. 3, lines 43-45), is removed following removal of the silicon nitride mask layer 53. Col. 3, lines 46-49 and 54-58.

It is respectfully submitted that there are at least three reasons that a *prima facie* case of obviousness has not been established against any of claims 1-4, 11-14, 16, 25-27, 33-35, or 37. By way of reminder, in determining whether a *prima facie* case of obviousness exists, the teachings of the references must be considered in their entireties. M.P.E.P. § 2141.02.

It is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine teachings from Tsai and Lancaster in the manner that has been asserted. In particular, Lancaster teaches a transistor gate fabrication process in which trenches are lined with a sacrificial oxide 52a prior to removing a silicon nitride layer 53, whereas the teachings of Tsai are drawn to a process for forming a trench isolation structure which includes lining trenches side wall oxidation 39 to relieve defects that occur as the edges of the silicon nitride layer 34A are etched back (col. 3, lines 34-37). Although, according to the Office, the process of Lancaster would have been know at the time the process disclosed in Tsai was developed, Tsai teaches that, rather than lining the trenches before removing silicon nitride, the trenches are lined following etch-back of silicon nitride. Accordingly, the inventors of Tsai, who are presumably of at least ordinary skill in the art, did not consider pre-coating the trenches as an option at the time the application which ultimately issued as Tsai was filed. As such, before the earliest priority date

for the above-referenced application, one of ordinary skill in the art would not have been motivated to incorporate teachings from Lancaster into the process of Tsai.

Furthermore, the radical, complete silicon nitride removal process taught in Lancaster would likely damage the silicon substrate and, therefore, requires protection of the substrate (with sacrificial oxide 52a) prior to removing the silicon nitride film 53. The number of defects that occur in the descuming process taught in Tsai, in which very small portions of the silicon nitride layer are removed, is correspondingly small. As the subsequent formation of side wall oxidation on the walls of trenches formed in the silicon substrate is sufficient to relieve these defects, one or ordinary skill in the art (including Tsai) would see no reason to form the side wall oxidation 39 before the descuming process.

Moreover, by teaching the complete removal of a silicon nitride layer before forming a transistor gate structure therein, Lancaster teaches away from a method in which portions of a silicon nitride layer remain as dielectric material is introduced into a trench to form an isolation structure therein, as recited in claims 1-4, 11-14, 16, 25-27, 33-35, and 37.

Additionally, it is respectfully submitted that the references teach away from the asserted combination. Lancaster teaches complete removal of a silicon nitride layer prior to filling trenches. This teaching is inconsistent with Tsai's teaching that a silicon nitride layer remain in place until after trenches are filled to "act[] as an end point detecting layer during [a] CMP process" in which dielectric, trench-filling material that overlies the plane of the silicon nitride layer is removed. Tsai, col. 3, lines 51-56; FIG. 3G.

Therefore, it does not appear that, without improper reliance upon the hindsight provided by the disclosure and claims of the above-referenced application, one of ordinary skill in the art would have been motivated to combine teachings from Tsai and Lancaster in the manner that has been asserted.

It is, therefore, respectfully submitted that the teachings of Tsai and Lancaster do not support a *prima facie* case of obviousness against any of claims 1-4, 11-14, 16, 25-27, 33-35, or 37. Accordingly, under 35 U.S.C. § 103(a), each of these claims is drawn to subject matter which is allowable over the teachings of Tsai and Lancaster, taken either separately or together.

Tsai, Lancaster, and the Examiner's Comment

Claims 17 and 38 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is allegedly unpatentable over that taught in Tsai, in view of the teachings of Lancaster and, further, in view of the Examiner's Comment.

Claim 17 is allowable, among other reasons, for depending indirectly from claim 11, which is allowable.

Claim 38 is allowable, among other reasons, for depending indirectly from claim 33, which is allowable.

Tsai, Lancaster, and Lee

Claims 5, 15, 28, and 36 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over that the subject matter taught in Tsai, in view of teachings from Lancaster and, further, in view of the teachings of Lee, HS, et al., "An Optimized Densification of the Filled Oxide for Quarter Micron Shallow Trench Isolation (STI)," 1996 IEEE Symposium on VLSI Technol. Dig. of Technical Papers, pages 158-59.

Claims 5, 15, 28, and 36 are allowable, among other reasons, for depending directly from claims 1, 11, 25, and 33, respectively, which are allowable.

CONCLUSION

It is respectfully submitted that each of claims 1-5, 11-17, 25-28, and 33-38 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,

Brick G. Power
Registration No. 38,581
Attorney for Applicants
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: August 10, 2005
BGP/djp:eg
Document in ProLaw